



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56, §1.97, and §1.98 PTO-1449 FORM	ATTORNEY DOCKET NO.: 38203-6079	SERIAL NO.: 10/039,426
	APPLICANTS: McArthur <i>et al.</i>	
Sheet 1 of 2	FILING DATE: January 4, 2002	GROUP ART UNIT: 2854 1756

U.S. PATENT DOCUMENTS

† EX'R INITIAL	*REF. #	PATENT NUMBER	DATE	NAME	U.S. CLASS/ SUBCLASS	FILING DATE (If appropriate)
Cuy	A	5,828,455	10/27/98	Smith <i>et al.</i>	356/354	3/07/97
	B	5,828,955	10/27/98	Smith <i>et al.</i>	455/324	8/30/95
Cuy	C	5,978,085	11/02/99	Smith <i>et al.</i>	356/354	10/23/97
Cuy	D	6,143,621	11/07/00	Tzeng <i>et al.</i>	438/401	6/14/99

FOREIGN PATENT DOCUMENTS

† EX'R INITIAL	*REF. #		TRANSLATION (YES/NO)

OTHER DOCUMENTS

† EX'R INITIAL	*REF. #	CITATION (Author, Article Title, Journal/Book Title, Date, Pertinent Pages, etc.)
Cuy	E	Hasan <i>et al.</i> , "Automated Electrical Measurements of Registration Errors in Step-and-Repeat Optical Lithography Systems", <i>IEEE Transactions on Electron Devices</i> , ED27(12):2304-2312 (1980)
Cuy	F	KLA 5105, "Linewidth and Misregistration System", KLA 5105 Product Specification, KLA Instruments Corporation, 2 pages (1995)
Cuy	G	KLA 5200, "Value-added Overlay Metrology for Advanced Lithography", KLA 5200 Product Specifications, KLA Instruments Corporation, 2 pages, (1996)
Cuy	H	Kodama <i>et al.</i> , "Measuring System XY-5i", <i>SPIE</i> , 2439:144-155 (1995)
Cuy	I	McFadden <i>et al.</i> , "A Computer Aided Engineering Workstation for Registration Control", <i>SPIE</i> , 1087:255-266 (1989)

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EXAMINER'S SIGNATURE 	SEP 16 2002 TC 1700	DATE CONSIDERED 9/03
† EXAMINER: Initial if reference is considered, whether or not citation is in conformance with MPEP 609. Line through citation if not in conformance and not considered. Include copy of this form in next communication to applicant. * If an asterisk is placed beside the reference number, a copy is not provided because the reference was previously cited by or submitted to the PTO in a prior application that is identified in the statement and relied upon for an earlier filing date under 35 U.S.C. 120. 37 C.F.R. 1.98(d).		



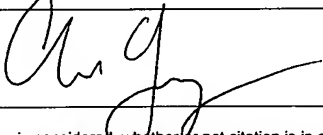
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<i>Cuz</i>	J	Pellegrini <i>et al.</i> , "Super Sparse Overlay Sampling Plans: An Evaluation of Methods and Algorithms for Optimizing Overlay Quality Control and Metrology Tool Throughput", <i>SPIE</i> , <u>3677</u> :72-82 (1999)
<i>Cuz</i>	K	Preil <i>et al.</i> , "A New Approach to Correlating Overlay and Yield", <i>SPIE</i> , <u>3677</u> :208-216 (1999)
<i>Cuz</i>	L	Sullivan, N.T., "Semiconductor Pattern Overlay", <i>SPIE Critical Reviews of Optical Science and Technology</i> , <u>CR52</u> :160-188 (1994)
<i>Cuz</i>	M	van den Brink <i>et al.</i> , "Direct-Referencing Automatic Two-Points Reticle-to-Wafer Alignment Using a Projection Column Servo System", <i>SPIE</i> , <u>633</u> :60-71 (1986)
<i>Cuz</i>	N	van den Brink <i>et al.</i> , "Matching of Multiple Wafer Steppers for 0.35 μ m Lithography Using Advanced Optimization Schemes", <i>SPIE</i> , <u>1926</u> :188-207 (1993)

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